```
=> d his full

     (FILE 'HOME' ENTERED AT 17:32:30 ON 11 MAY 2001)

     FILE 'USPATFULL' ENTERED AT 17:32:41 ON 11 MAY 2001
L1          260 SEA (MULTIPL? OR PLURAL? OR SECOND OR AUXILIARY OR DUAL OR
TWO
                OR BOTH OR ALTERNATE)(6A)(PREFETCH(2W)(BUFFER# OR REGISTER#
OR
                UNIT#))
L2           28 SEA L1(P)SIZE
L3            0 SEA L1(P)AGE
L4           18 SEA L1(P)VALID?
L5            1 SEA L4(P)SIZE
                D L5 PH,HIT
                D L5 PN,HIT
L6           21 SEA (SIZE (P) AGE (P) VALID?)(P)(DATA OR OPERAND)
                D L6 1-21 PN,TI,HIT
                SET LINELENGTH 80
```

(FILE 'HOME' ENTERED AT 16:39:39 ON 11 MAY 2001)

FILE 'USPATFULL' ENTERED AT 16:39:46 ON 11 MAY 2001

L1	1377	S	INSTRUCTION#(6A)ALIGN?
L2	300	S	L1(P)PREFETCH?
L3	613	S	PREFETCH?(P)(VALID? OR INVALID?)
L4	48	S	L3(P)(SIZE OR CAPACITY)
L5	22	S	L4(P)INSTRUCTION#

PI US 5404560 19[illegible]0404
TI Microprocessor [illegible]ving external control store
IN Lee, Raymond Y., Salem, NH, United States
Bessolo, Jeffrey M., Groton, MA, United States
Shah, Vyomesh, Tewksbury, MA, United States
Vincelette, Scott D., Bethlehem, PA, United States
Waldstein, Steven M., Westford, MA, United States
Nathan, Jeffrey D., Andover, MA, United States
Lang, Steven E., Lincoln Center, MA, United States

L8 ANSWER 19 OF 20 USPATFULL
PI US 5367657 19941122
TI Method and apparatus for efficient read prefetching of instruction code data in computer memory subsystems
IN Khare, Manoj, Fremont, CA, United States
Cadambi, Sudarshan B., Portland, OR, United States

L8 ANSWER 20 OF 20 USPATFULL
PI US 5345560 19940906
TI Prefetch buffer and information processing system using the same
IN Miura, Shuuichi, 313 Izumigamoriryo, 20-1, Mizukicho 2-chome, Hitachi-shi, Ibaraki-ken, Japan
Kurosawa, Kenichi, 22-2, Mikanoharacho 2-chome, Hitachi-shi, Ibaraki-ken, Japan
Nakamikawa, Tetsuaki, 17-1-402, Moriyamacho 3-chome, Hitachi-shi, Ibaraki-ken, Japan
Hirose, Kenji, 17-11-205, Hidakacho 5-chome, Hitachi-shi, Ibaraki-ken, Japan

L8 ANSWER 1 OF 20 USPATFULL
PI US 6202142 20010313
TI Microcode scan unit for scanning microcode instructions using predecode data
IN Narayan, Rammohan, Austin, TX, United States
Southard, Shane A., Austin, TX, United States
Tran, Thang M., Austin, TX, United States

L8 ANSWER 2 OF 20 USPATFULL
PI US 6122729 20000919
TI Prefetch buffer which stores a pointer indicating an initial predecode position
IN Tran, Thang M., Austin, TX, United States

L8 ANSWER 3 OF 20 USPATFULL
PI US 5996071 19991130
TI Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address
IN White, Christopher E., Dallas, TX, United States
Fourcroy, Antone L., Fort Collins, CO, United States

L8 ANSWER 4 OF 20 USPATFULL
PI US 5995743 19991130
TI Method and system for interrupt handling during emulation in a data processing system
IN Kahle, James Allan, Austin, TX, United States
Mallick, Soummya, Austin, TX, United States

L8 ANSWER 5 OF 20 USPATFULL
PI US 5968163 19991019
TI Microcode scan unit for scanning microcode instructions using predecode data
IN Narayan, Rammohan, Austin, TX, United States
Southard, Shane A., Austin, TX, United States
Tran, Thang M., Austin, TX, United States

L8 ANSWER 6 OF 20 USPATFULL
PI US 5953520 19990914
TI Address translation buffer for data processing system emulation mode
IN Mallick, Soummya, Austin, TX, United States

L8 ANSWER 7 OF 20 USPATFULL
PI US 5944815 19990831
TI Microprocessor configured to execute a prefetch instruction including an
access count field defining an expected number of access
IN Witt, David B., Austin, TX, United States

L8 ANSWER 8 OF 20 USPATFULL
PI US 5909566 19990601
TI Microprocessor circuits, systems, and methods for speculatively executing an instruction using its most recently used data while concurrently prefetching data for the instruction
IN Cai, George Z. N., Plano, TX, United States
Shiell, Jonathan H., Plano, TX, United States

L8 ANSWER 9 OF 20 USPATFULL
PI US 5854911 19981229
TI Data buffer prefetch apparatus and method
IN Watkins, John E., Sunnyvale, CA, United States

L8 ANSWER 10 OF 20 USPATFULL
PI US 5852727 19981222
TI Instruction scanning unit for locating instructions via parallel scanning of start and end byte information
IN Narayan, Rammohan, Austin, TX, United States
Tran, Thang M., Austin, TX, United States

L8 ANSWER 11 OF 20 USPATFULL
PI US 5850532 19981215
TI Invalid instruction scan unit for detecting invalid predecode data corresponding to instructions being fetched
IN Narayan, Rammohan, Austin, TX, United States
Southard, Shane A., Austin, TX, United States
Tran, Thang M., Austin, TX, United States

L8 ANSWER 12 OF 20 USPATFULL
PI US 5845101 19981201
TI Prefetch buffer for storing instructions prior to placing the instructions in an instruction cache
IN Johnson, William M., Austin, TX, United States
Tran, Thang M., Austin, TX, United States
Gavin, Matt T., Austin, TX, United States
Pedneau, Mike, Austin, TX, United States

L8 ANSWER 13 OF 20 USPATFULL
PI US 5761706 19980602
TI Stream buffers for high-performance computer memory system
IN Kessler, Richard E., Eau Claire, WI, United States
Oberlin, Steven M., Chippewa Falls, WI, United States
Scott, Steven L., Eau Claire, WI, United States
Palacharla, Subbarao, Madison, WI, United States

L8 ANSWER 14 OF 20 USPATFULL
PI US 5734881 19980331
TI Detecting short branches in a prefetch buffer using target location information in a branch target cache
IN White, Christopher E., Dallas, TX, United States
Fourcroy, Antone L., Fort Collins, CO, United States
McDermott, Mark W., Austin, TX, United States

L8 ANSWER 15 OF 20 USPATFULL
PI US 5701448 19971223
TI Detecting segment limit violations for branch target when the branch unit does not supply the linear address
IN White, Christopher E., Dallas, TX, United States

L8 ANSWER 16 OF 20 USPATFULL
PI US 5680564 19971021
TI Pipelined processor with two tier prefetch buffer structure and method with bypass
IN Divivier, Robert James, San Jose, CA, United States
Nemirovsky, Mario, San Jose, CA, United States

L8 ANSWER 17 OF 20 USPATFULL
PI US 5566324 19961015
TI Computer apparatus including a main memory prefetch cache and method of operation thereof
IN Kass, William J., Easley, SC, United States

L8 ANSWER 18 OF 20 USPATFULL

L5 ANSWER 1 OF 22 USPATFULL
PI US 6175898 20010116
TI Method for prefetching data using a micro-TLB
IN Ahmed, Sultan, Santa Clara, CA, United States
Chamdani, Joseph, Santa Clara, CA, United States

L5 ANSWER 2 OF 22 USPATFULL
PI US 6161208 20001212
TI Storage subsystem including an error correcting cache and means for performing memory to memory transfers
IN Dutton, Patrick Francis, Apalachin, NY, United States
Gregor, Steven Lee, Endicott, NY, United States
Li, Hehching Harry, Endicott, NY, United States

L5 ANSWER 3 OF 22 USPATFULL
PI US 5867683 19990202
TI Method of operating a high performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations
IN Witt, David B., Austin, TX, United States
Johnson, William M., Austin, TX, United States

L5 ANSWER 4 OF 22 USPATFULL
PI US 5867682 19990202
TI High performance superscalar microprocessor including a circuit for converting CISC instructions to RISC operations
IN Witt, David B., Austin, TX, United States
Johnson, William M., Austin, TX, United States

L5 ANSWER 5 OF 22 USPATFULL
PI US 5848432 19981208
TI Data processor with variable types of cache memories
IN Hotta, Takashi, Hadano, Japan
Kurihara, Toshihiko, Hadano, Japan
Tanaka, Shigeya, Hitachi, Japan
Sawamoto, Hideo, Machida, Japan
Osumi, Akiyoshi, Hitachi, Japan
Saito, Koji, Hadano, Japan
Shimamura, Kotaro, Hitachi, Japan

L5 ANSWER 6 OF 22 USPATFULL
PI US 5805853 19980908
TI Superscalar microprocessor including flag operand renaming and forwarding apparatus
IN White, Scott A., Austin, TX, United States
Christie, David S., Austin, TX, United States
Goddard, Michael D., Austin, TX, United States

L5 ANSWER 7 OF 22 USPATFULL
PI US 5784590 19980721
TI Slave cache having sub-line valid bits updated by a master cache
IN Cohen, Earl T., Fremont, CA, United States
Pattin, Jay C., Redwood City, CA, United States

L5 ANSWER 8 OF 22 USPATFULL
PI US 5751981 19980512
TI High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a

variable byte-length format
IN Witt, David B., Austin, TX, United States
Johnson, William M., Austin, TX, United States

L5 ANSWER 9 OF 22 USPATFULL
PI US 5724422 19980303
TI Encrypting and decrypting instruction boundaries of instructions in a superscalar data processing system
IN Shang, Shisheng, Kaohsiung, Taiwan, Province of China
Chang, Chung-Chih, Yun-Lin, Taiwan, Province of China
Hsu, Chia-Chang, Tainan, Taiwan, Province of China

L5 ANSWER 10 OF 22 USPATFULL
PI US 5664136 19970902
TI High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations
IN Witt, David B., Austin, TX, United States
Johnson, William M., Austin, TX, United States

L5 ANSWER 11 OF 22 USPATFULL
PI US 5655098 19970805
TI High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format
IN Witt, David B., Austin, TX, United States
Johnson, William M., Austin, TX, United States

L5 ANSWER 12 OF 22 USPATFULL
PI US 5655097 19970805
TI High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format
IN Witt, David B., Austin, TX, United States
Johnson, William M., Austin, TX, United States

L5 ANSWER 13 OF 22 USPATFULL
PI US 5651125 19970722
TI High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations
IN Witt, David B., Austin, TX, United States
Johnson, William M., Austin, TX, United States

L5 ANSWER 14 OF 22 USPATFULL
PI US 5632023 19970520
TI Superscalar microprocessor including flag operand renaming and forwarding apparatus
IN White, Scott A., Austin, TX, United States
Christie, David S., Austin, TX, United States
Goddard, Michael D., Austin, TX, United States

L5 ANSWER 15 OF 22 USPATFULL
PI US 5581774 19961203
TI Data processor decoding and executing a train of instructions of variable length at increased speed
IN Yoshitake, Akihiro, Kawasaki, Japan
Ohshima, Toshiharu, Kawasaki, Japan

L5 ANSWER 16 OF 22 USPATFULL
PI US 5551001 19960827
TI Master-slave cache system for instruction and data cache memories
IN Cohen, Earl T., Fremont, CA, United States
Tilleman, Russell W., Palo Alto, CA, United States
Pattin, Jay C., Redwood City, CA, United States
Blomgren, James S., San Jose, CA, United States

L5 ANSWER 17 OF 22 USPATFULL
PI US 5509130 19960416
TI Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor
IN Trauben, Richard D., Morgan Hill, CA, United States
Nanda, Sunil, Los Altos, CA, United States

L5 ANSWER 18 OF 22 USPATFULL
PI US 5455955 19951003
TI Data processing system with device for arranging instructions
IN Kida, Hiroyuki, Hitachi, Japan
Maejima, Hideo, Hitachi, Japan
Masuda, Ikuro, Hitachi, Japan
Baba, Shirou, Tokorozawa, Japan

L5 ANSWER 19 OF 22 USPATFULL
PI US 5276848 19940104
TI Shared two level cache including apparatus for maintaining storage consistency
IN Gallagher, Patrick W., Vestal, NY, United States
Gregor, Steven L., Endicott, NY, United States
Reeve, Stephen M., Endicott, NY, United States

L5 ANSWER 20 OF 22 USPATFULL
PI US 5243705 19930907
TI System for rapid return of exceptional processing during sequence operation instruction execution
IN Nakagawa, Teruo, Aichi, Japan

L5 ANSWER 21 OF 22 USPATFULL
PI US 5170476 19921208
TI Data processor having a deferred cache load
IN Laakso, Pamela S., Austin, TX, United States
Martin, Bradley, Austin, TX, United States

L5 ANSWER 22 OF 22 USPATFULL
PI US 4992932 19910212
TI Data processing device with data buffer control
IN Ohshima, Toshiharu, Kawasaki, Japan